

FT2232HL Breakout Board

Hardware Reference

Rev. 1r0

FT2232HL is literally a USB to everything bridge. It's a USB 2.0 conversion chip that can function as (when connected to a PC)

- Two Channel UART
- JTAG
- SPI
- I2C
- Parallel I/O

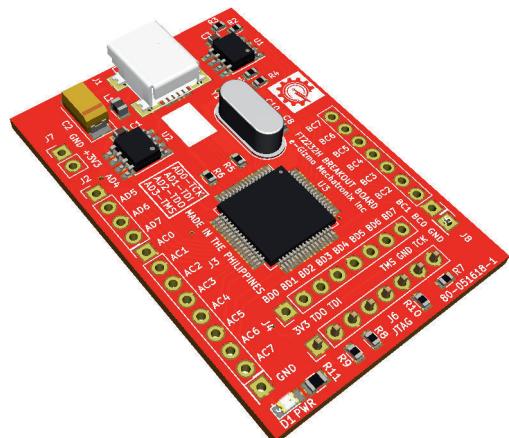
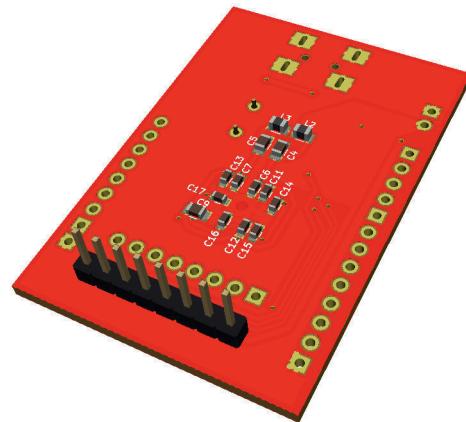
FTDI provides all the necessary USB drivers needed to make the chip work on various OS, including Windows, Linux, and Android(J2XX). DLL is even available for free to enable users to build their own apps that can access the full functional capability of the FT2232HL.

This breakout board was designed with the LCMX02 FPGA kit in mind - as a full function JTAG programmer (J6 JTAG port). I/Os assigned to this port can be used for other purpose if this feature is not used.

An on board 3.3V low dropout voltage regulator is provided. The 3.3V can source up to 150mA, and is short circuit protected. All FT2232HL I/O pins are accessible through a set of 2.54 mm pitch mounting holes. You can install appropriately sized connectors of your preference (e.g. pin headers or sockets) on these mounting locations. These are also spaced to allow mounting to 2.54mm pitch prototyping boards.

Download the FT2232HL datasheet for a detailed description and usage of this chip.

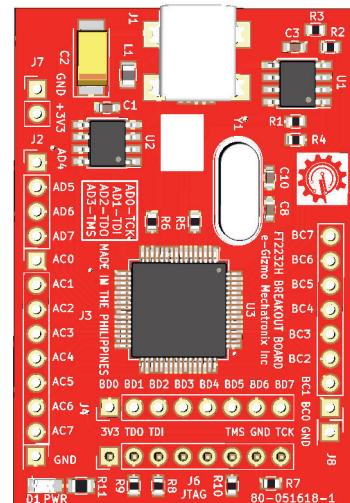
https://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232H.pdf



PIN FUNCTION MAP

Following is a quick reference guide for the I/O pin functions. This table is taken wholly from FTDI's FT2232H datasheet. Note that each pins takes a different personality depending on the device configuration you selected. Always consult the device datasheet for more details.

Note further that due to limited PCB space, the pin names printed on the PCB are truncated as follows: **ADBUSHx** = **ADx**, **BDBUSHx** = **BDx**, and **BCBUSx** = **BCx**. For example, ADBUS7 is labeled as AD7 in the PCB.



FT2232HL and FT2232HQ (64-pin)										
Pin		Pin functions (depends on configuration)								
Pin #	Pin Name	ASYNC Serial (RS232)	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	Host Bus Emulation
Channel A										
16	ADBUSH0	TXD	D0	D0	D0	D0	TCK/SK	USES	D0	AD0
17	ADBUSH1	RXD	D1	D1	D1	D1	TDI/DO		D1	AD1
18	ADBUSH2	RTS#	D2	D2	D2	D2	TDO/DI		D2	AD2
19	ADBUSH3	CTS#	D3	D3	D3	D3	TMS/CS		D3	AD3
21	ADBUSH4	DTR#	D4	D4	D4	D4	GPIOLO0		D4	AD4
22	ADBUSH5	DSR#	D5	D5	D5	D5	GPIOLO1		D5	AD5
23	ADBUSH6	DCD#	D6	D6	D6	D6	GPIOLO2		D6	AD6
24	ADBUSH7	RI#	D7	D7	D7	D7	GPIOLO3		D7	AD7
26	ACBUS0	TXDEN	RXF#	RXF#	**	**	GPIOHO0		CS#	A8
27	ACBUS1	**	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1		A0	A9
28	ACBUS2	**	RD#	RD#	RDSTB#	RDSTB#	GPIOH2		RD#	A10
29	ACBUS3	RXLED#	WR#	WR#	**	**	GPIOH3		WR#	A11
30	ACBUS4	TXLED#	SIWUA	SIWUA	SIWUA	SIWUA	GPIOH4		SIWUA	A12
32	ACBUS5	**	CLKOUT	**	**	**	GPIOH5		**	A13
33	ACBUS6	**	OE#	**	**	**	GPIOH6		**	A14
34	ACBUS7	**	**	**	**	**	GPIOH7		**	A15
Channel B										
38	BDBUSH0	TXD		D0	D0	D0	TCK/SK	FSDI	D0	CS#
39	BDBUSH1	RXD		D1	D1	D1	TDI/DO	FSCLK	D1	ALE
40	BDBUSH2	RTS#		D2	D2	D2	TDO/DI	FSDO	D2	RD#
41	BDBUSH3	CTS#		D3	D3	D3	TMS/CS	FSCTS	D3	WR#
43	BDBUSH4	DTR#		D4	D4	D4	GPIOLO0		D4	IORDY
44	BDBUSH5	DSR#		D5	D5	D5	GPIOLO1		D5	CLKOUT
45	BDBUSH6	DCD#		D6	D6	D6	GPIOLO2		D6	I/O0
46	BDBUSH7	RI#		D7	D7	D7	GPIOLO3		D7	I/O1
48	BCBUS0	TXDEN	RXF#	**	**	**	GPIOHO0		CS#	**
52	BCBUS1	**	TXE#	WRSTB#	WRSTB#	WRSTB#	GPIOH1		A0	**
53	BCBUS2	**	RD#	RDSTB#	RDSTB#	RDSTB#	GPIOH2		RD#	**
54	BCBUS3	RXLED#		WR#	**	**	GPIOH3		WR#	**
55	BCBUS4	TXLED#		SIWUB	SIWUB	SIWUB	GPIOH4	SIWUB	SIWUB	**
57	BCBUS5	**		**	**	**	GPIOH5		**	**
58	BCBUS6	**		**	**	**	GPIOH6		**	**
59	BCBUS7	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	GPIOH7	PWRSAV#	PWRSAV#	PWRSAV#
60	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#
36	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #
Configuration memory interface										

